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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/707,892	01/21/2004	Tien-Jen Cheng	FIS920030352US1	1891

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EXAMINER
LANDAU, MATTHEW C

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 09/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)	
	10/707,892	CHENG ET AL.	
	Examiner	Art Unit	
	Matthew Landau	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *15-20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 January 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/21/04, 2/2/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Applicant's election without traverse of Group I, claims 1-14, in the reply filed on 7/18/2005, is acknowledged.

Claims 15-20 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim.

Drawings

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the hard test barrier comprising a copper layer (claim 6) must be shown or the feature(s) canceled from the claim(s). Also, the plurality of identical ICs on a wafer, each of said plurality of identical ICs located in a die on said wafer (claim 14) must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the

renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

Claims 1, 8, and 9 are objected to because of the following informalities:

Regarding claim 1, there is insufficient antecedent basis in the claim for the limitations "said terminal metallurgy" and "said conducting barrier layer". Furthermore, it appears that a semicolon is missing after the limitation "a conducting layer on said diffusion barrier".

Regarding claim 8, there is insufficient antecedent basis in the claim for the limitations "said terminal metallurgy" and "said diffusion barrier layer".

Regarding claim 9, there is insufficient antecedent basis in the claim for the limitation "said adhesion/diffusion barrier layer".

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who

> has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

Claims 1-5 and 7 are rejected under 35 U.S.C. 102(e) as being anticipated by Homma et al. (US Pat. 6,798,050, hereinafter Homma).

Regarding claim 1, Figure 9E of Homma discloses a chip pad comprising: a terminal metal layer 81 disposed on a passivating layer 82, a diffusion barrier layer 84/85 on said terminal metallurgy; a conducting layer 86 on said diffusion barrier; a hard test barrier 87 (Pd) on said conducting layer; and a plate passivating layer 89 on said hard test barrier layer.

Regarding claims 2-4, Figure 9E of Homma discloses said diffusion barrier layer 84/85 includes an adhesion layer 85 (Ti) on barrier metallurgy 84 (TiN) (col. 11, lines 12-15).

Regarding claims 1, 5, and 7 (as an alternate interpretation), Figure 9E of Homma discloses a chip pad comprising: a terminal metal layer 81 disposed on a passivating layer 82, a diffusion barrier layer 84 on said terminal metallurgy; a conducting layer 85 on said diffusion barrier; a hard test barrier 86 (Ni) on said conducting layer; and a plate passivating layer 87 (Au) on said hard test barrier layer (col. 11, lines 20-23).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1 and 5-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tseng et al. (US Pat. 6,696,356, hereinafter Tseng) in view of McCormick (US Pat. 6,706,622).

Regarding claims 1 and 5-7, Figure 3F of Tseng discloses a chip pad comprising: a terminal metal layer 15 disposed on a passivating layer 14, a diffusion barrier layer 18 on said terminal metallurgy; a conducting layer 20 on said diffusion barrier; a hard test barrier 28/26 (Ni/Cu) on said conducting layer (col. 10, lines 24-28). The difference between Tseng and the claimed invention is a gold plate passivating layer formed on said hard test barrier. Figure 6 of McCormick discloses a bonding pad with a gold passivating layer 30 over a nickel layer 26. In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made to modify the invention of Tseng by including a gold layer above the hard test barrier for the purpose of inhibiting oxidation of the nickel layer (col. 3, lines 41-43 of McCormick).

Claims 8-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Degani et al. (US Pat. 6,232,212, hereinafter Degani) in view of McCormick.

Regarding claims 8 and 11-13, Figures 1 and 9 of Degani discloses an IC chip 11 with a chip pad formed thereon comprising: a terminal metal layer 13 disposed on a chip passivating layer 12 and connecting to underlying chip wiring through a via through said chip passivating layer; an adhesion/barrier layer 22/21 on said terminal metal layer; a seed layer 23 (Cu) (col. 3, line 53) on said adhesion/barrier layer; and a plate passivating layer 24 (Au) (col. 3, line 63). The difference between Degani and the claimed invention is a hard test barrier layer (made of nickel) on said diffusion barrier layer. Figure 6 of McCormick discloses a bond pad structure with a nickel layer 26 between a copper layer 20 and an overlying gold layer 30. In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made

to modify the invention of Degani by including a nickel hard test barrier layer as taught by McCormick for the purpose of isolating the copper from other material which may degrade the copper, or which may be degraded by the copper (col. 2, lines 5-9 of McCormick). Note that it is considered to be inherent to have a plurality of chip interconnect pads on an IC chip. Assuming, *arguendo*, that it is not inherent to have more than one pad on an IC chip, it would certainly be obvious to modify Degani to have more than one pad as taught by McCormick (Figure 6) for the purpose of allowing separate electrical connections to different portions of the integrated circuit.

Regarding claims 9 and 10, Degani discloses said adhesion/diffusion barrier layer includes an adhesion layer 22 (CrCu) on a barrier metallurgy 21 (Ti) (col. 3, lines 41-48).

Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Degani in view of McCormick as applied to claim 13 above, and further in view of Homma and Bhattacharya et al. (US PGPub 2003/0034489, hereinafter Bhatt).

Regarding claim 14, semiconductor IC chips are fabricated from a wafer of semiconductor material, and the wafer is not diced into individual chips until after the ICs have been completed. Therefore, in order to make the device of Degani, there must have been a plurality of IC chips on a wafer at an intermediate stage of processing. However, Degani does not explicitly disclose that the wafer is diced into individual IC chips after forming the claimed metal layers on the IC chip substrate. Figures 9A-9E of Homma discloses forming a plurality of metal layers on a wafer prior to dicing the wafer into individual chips (col. 11, lines 38-41). In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made to further modify the invention of Degani by dicing the wafer after forming

the claimed metal layers, thereby resulting in a plurality of ICs (with the claimed structure) on a wafer. The ordinary artisan would have been motivated to further modify Degani in the manner described above for the purpose of simply the production process for mass production. A further difference between Degani and the claimed invention is the ICs are identical. Bhatt discloses forming a plurality of identical ICs on a wafer (paragraph [0030]). In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made to further modify the invention of Degani by having a plurality of identical ICs on a wafer for the purpose of simplifying the production process for mass production of a particular IC. Note that paragraph [0003] of the instant application gives a special definition to the word "die" by stating "Each array location is known as a die and each die may harbor an IC chip". In other words, a "die" is simply the portion of the wafer where the chip is located. Therefore, it is inherent that each of said plurality of identical ICs are located in a die on said wafer.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew C. Landau whose telephone number is (571) 272-1731.

The examiner can normally be reached from 8:30 AM - 5:30 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone numbers for the organization where this application or proceeding is assigned are (571) 273-8300 for regular communications and (571) 273-8300 for After Final communications.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should any questions arise regarding access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Matthew C. Landau

September 4, 2005